

## CLAIMS:

1 A VLSI circuit for implementing in hardware any multiple output combinational circuit having the output functions expressed in logical sum-of-product equations, with  $m$  inputs,  $r$  outputs and  $n$  product terms  $p(k)$ , comprising:

a register with  $m$  bits for storing the input variables;

$n$  cells, a cell  $C(k)$  for determining the logical value of a product term  $p(k)$  of said equations for given inputs;

a logical summing circuit, realised with  $r$  OR gates each one with  $n$  inputs, associated with said cell  $C(k)$  for receiving the logical value of product terms  $p(k)$  and outputting the  $r$  bits of output functions.

2 A VLSI circuit as defined in claim 1, wherein said cell  $C(k)$  comprises:

a storage area for storing the information that characterize a product term, named mask word, product word and function word;

first AND gates means for receiving said inputs and said mask word to produce a first intermediate result, which identify the input variables that form a product term;

EQUIVALENCE gates means for comparing the said product term with said first intermediate result to produce a second intermediate result concerning a product term;

second AND gate means for receiving the said second intermediate result to produce a logical value which is the value of the product term; if this value is logical 1 the product term is active;

third AND gates means to allow passing said function word if said product term is active, and consequently to be OR-ed with function words of other active product terms.

3 A cell  $C(k)$  as defined in claim 2, wherein said storage area of a cell  $C(k)$  comprises three  $m$ -bit registers for  $m$  input bits of said  $C(k)$  cell.

4 A cell C(k) as defined in claim 2, wherein said first AND gates of a cell C(k) comprises m 2-bit AND gates to produce said first intermediate result for m input bits.

5 A cell C(k) as defined in claim 2, wherein said EQUIVALENCE gates of a cell C(k) comprises m 2-bit EQUIVALENCE (XOR) gates to produce said second intermediate result for m input bits.

6 A cell C(k) as defined in claim 2, wherein said second AND gate of a cell C(k) comprises one m-bit AND gate to produce a logical value which is the value of the product term for m input bits.

7 A cell C(k) as defined in claim 2, wherein said third AND gates of a cell C(k) comprises m 2-bit AND gates to allow passing said function word if said product term has the logical value of 1, for m input bits.

8 A VLSI circuit according to claim 2 for implementing in hardware any synchronous sequential circuit with clock input only and outputs taken from the state register, having the next state functions expressed in logical sum-of-product equations, with m bits in state register and n product terms p(k), further comprising:

a clock input;

a state register with m bits for storing the state variables;

n cells of said cell C(k) for determining the logical value of a product term p(k) of said next state equations;

a logical summing circuit, realised with m OR gates each one with n inputs, associated with said cell C(k) for receiving the logical value of product terms p(k) and outputting the m bits of said next state functions;

a feedback connection to establish the next state.

9 A VLSI circuit according to claim 2 for implementing in hardware any synchronous sequential circuit with data inputs and clock input, having the next state functions and the output functions expressed in logical sum-of-product equations, with m inputs, r outputs, s bits in state register, n1 product terms p(k) in next state equations and n2 product terms p(k) in output equations, further comprising:

a clock input;

a register with  $m$  bits for storing the input variables;

a state register with  $s$  bits for storing the state variables;

$n1$  cells of said cell  $C(k)$  for determining the logical value of a product term  $p(k)$  of said next state equations;

$n2$  cells, said cell  $C(k)$  for determining the logical value of a product term  $p(k)$  of said output equations;

a logical summing circuit, realised with  $(m + s)$  OR gates each one with  $n1$  inputs, associated with said cell  $C(k)$  for receiving the logical value of product terms  $p(k)$  of the next state equations and outputting the  $(m + s)$  bits of next state functions.

a logical summing circuit, realised with  $r$  OR gates each one with  $n2$  inputs, associated with said cell  $C(k)$  for receiving the logical value of product terms  $p(k)$  and outputting the  $r$  bits of output functions.

a feedback connection to establish the next state;

10 An expert system for interpreting and analysing the logical behaviour of digital circuits, given by input variables, outputs and logical equations in form of sum-of-products, where interpreting and analysing:

- means to validate said input variables and said outputs;
- means to analyse said logical equations;
- means to generate for every product term said mask word, said product word and said function word;
- means to transform the individual lists, generated for each product term in a single memory list defining the logical behaviour of a digital circuit and storing same in a database.

11 A method for dynamically configuring the logical behaviour of a VLSI circuit as described in claim 1, or a VLSI circuit as described in claim 8, or a VLSI circuit as described in claim 9, by performing the steps of:

inputting the input variables, the outputs and a plurality of sum-of-product equations, which describe the logical behaviour of a digital circuit, to an expert system as defined in claim 10;

generating three memory words uniquely defining each product term of said equations, as defined in claim 10; and

storing said mask word, said product word, and said function word into a corresponding register associated with a cell  $C(k)$ , as described in claim 2.

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